American University of Beirut
Department of Electrical and Computer Engineering
EECE 321L - Computer Organization Lab

Name: **ID:**
Partner's Name: **ID:**

Midterm

March 31, 2009

In the following, you have to write a VHDL code in order to implement a finite state machine. This machine behaves as a funny counter. Its count sequence is: 11, 91, 72, 63.
The separation between any two counts is six seconds. Also, design a 'Reset' button that takes the machine to its initial state; ie, 11. Make sure to include your clock counter mapping code. Finally, synthesize your code and implement it using the FPGA.
Write any comments or assumptions you come up with on this paper. Make sure to draw a state diagram of the FSM.

aha39@aub.edu.lb